A Compact Memory Structure based on 2T1R Against Single-Event Upset in RRAM Arrays

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Abstract

The single-event upset (SEU) has significant influence on the reliability of 1-transistor-1-RAM (1T1R) array due to heavy ion strikes. This paper proposes a compact memory structure based on 2-transistor-1-RRAM (2T1R), which exploits the signal space between adjacent cells in the RRAM array structure. Results show that the proposed structure can successfully alleviate the SEU effect in RRAM array – it eliminates the overhead of 1ns delay and 400pJ power consumption of READ operation, as well as 2ns delay of RESET operation, at the cost of only 1.9% area overhead compared to the 1T2R structure.

1. Introduction

Resistive random access memory (RRAM) device has become one of the most promising nonvolatile memories (NVM) for its simple structure and capability of integration with the silicon CMOS technology. Besides, it also has benefits of low programming voltage, fast switching speed, high ratio of different states and high endurance. The structure and I-V curve of RRAM are shown in Figure 1. Even though RRAM is immune to SEU as its intrinsic property, the soft errors may occur in the 1T1R cell due to the heavy ion strikes on the junction of MOSFET [1], as shown in Figure 2.

In order to mitigate the influence of SEU on cells in memory array circuits, new technologies, such as Fully-Depleted Silicon on Insulator (FD-SOI) [3] technology, have been proposed to improve the radiation resistance of the 1T1R cell. However, RRAM is still under threat of SEU, especially in the harsh environment of space. Therefore, it is still worth exploring further to avoid functional failure due to radiation. Tosson et al. proposed 1T2R structure [4] to fix the soft error by introducing the error detection process. In contrast, we propose a compact radiation hardening memory structure which can avoid the extra processes while mitigating the SEU influence.

2. The Proposed Compact Memory Structure

The memory structure based on 2T1R cells with independent signals is adopted to mitigate the SEU influence, as shown in Figure 3. Two transistors control RRAM device from both electrodes with the same WL signal. In this way, the potential SEU problem in cells shown in Figure 2 will be avoided.

However, the area of 2T1R cells with independent signals will increase about 40% compared with 1T2R [4] structure. To save the chip area while keeping the benefits of its intrinsic property, we propose a compact memory structure (see Figure 4) that can share respective BL and SL to take full advantage of the characteristics of the
2T1R cell. In this way, signal wires BL/SL will be shared by flipping the cells on their respective sides, which can effectively reduce the area cost (only 0.3% increase compared with the area of 1T2R) of diffusion intervals “d2” on the horizontal dimension. Of course, the proposed structure will introduce additional peripheral circuits between the column decoder and signals BL/SL. There are four kinds of cells being selected in both SET and RESET operations. For example, there are unselected cells, fully-select cell, half-select cell and vibratory cell in both operations. The corresponding voltage bias situation of the four kinds of cells are shown in Figure 5 (WEA/WEB will be introduced later). Besides, cells whose WLs are not activated in other rows will be isolated due to the benefits of 2T1R structure. However, the half-select cell is vulnerable to heavy ion strikes.

In order to lessen the SEU effect on 2T1R, two wires (WEA/WEB) connecting respective electrodes of RRAM are introduced (see Figure 4) by indirectly isolating the vulnerable junction and maintaining the potential. Four different situations of the biasing condition of WEA and WEB are illustrated in Figure 6. Besides, when the cell remains at unselected or vibratory selected condition, WEA/WEB will keep floating.

3. Modifications to the Column Decoder Circuitry

Shown in Figure 7, supplementary circuits are added between the column decoder and signals BL/SL to support the changes of operations in the 2T1R compact memory structure. Once the column address signal arrives, the Combination ADDR X/Y Units will merge the address into specific BL and SL signals in the separate operation of SET or RESET. After that, selection signals will be stabilized through the global and local drivers, which is typically used in a hierarchical design. Meanwhile, the selection signals from the global driver will be transferred to Mitigation Units as well. The Mitigation Units will set the appropriate bias voltage for the selected WEA and WEB against SEU in half-select and fully-select cells.
output states will not affect each other during the different operations of X/Y Units, avoiding wrong selections.

![Figure 8. Symbol/Schematic of ADDR X/Y Unit.](image)

Figure 8. Symbol/Schematic of ADDR X/Y Unit.

When the relevant half-select cell or fully-select cell is selected, one or both of the BL and SL signals will be at the high potential to activate the Mitigation Unit as shown in Figure 9 (WEA and WEB in (b) run through a column of the array). Considering the requirement of low power in design, transistors with high threshold voltage should be able to control the leakage current further. In order to demonstrate the sequence of operations for half-select case and fully-select case, the signal waveforms of SET operation are shown in Figure 10, and waveforms of the RESET Operation are similar.

![Figure 9. Symbol and Schematic of Mitigation Unit.](image)

Figure 9. Symbol and Schematic of Mitigation Unit.

4. Simulation Results

The simulation setup in our work is based on [2, 5]. A SPICE model describing the RRAM devices in [6] is adopted to evaluate the performance of a RRAM array. Since the difference in RRAM device organization and voltage bias will cause the various HRS-LRS resistance range, we use the same voltage profile as in [4]. The photocurrent model [1] is used to evaluate the current at the MOSFET junction caused by heavy ion strikes.

![Figure 10. Waveforms of the SET Operation Signals for Half-select / Fully-select Cells.](image)

The simulation results (see Figure 11) show that spurious HRS to LRS transitions may occur in a half-select cell with 1T1R like structure during SET/RESET operation. However, 2T1R structure can successfully alleviate the SEU influence on the potential difference between two electrodes of RRAM to protect the stored data.

![Figure 11. Comparisons between the SEU influence on 1T1R Like Structure and the Proposed One.](image)

In order to demonstrate the performance of the proposed structure, we firstly detail the energy comparison in write operation for the memory structure of 1T2R [4], 2T1R with independent signals, and proposed 2T1R with shared signals as shown in Table 1.

Then we compare the area and write operation energy using CACTI [7]. Figure 12 shows the simulation results of four structures in the chip area and the relative growth rate based on the profile of 1T1R. The relative growth of the structure of 1T2R will increase by about 53.4%.
Table 1. Energy in Write Operation for 1T1R, 1T2R, 2T1R (Independent Signals) and 2T1R (Shared Signals) 128 × 128 Array.

<table>
<thead>
<tr>
<th>Operation</th>
<th>1T1R</th>
<th>1T2R [4]</th>
<th>2T1R Independent</th>
<th>2T1R Shared</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set</td>
<td>665.75</td>
<td>644.42</td>
<td>(−3.30%)</td>
<td>706.65</td>
</tr>
<tr>
<td>Reset</td>
<td>106.51</td>
<td>115.11</td>
<td>(8.11%)</td>
<td>278.96</td>
</tr>
</tbody>
</table>

Meanwhile, 2T1R with shared signals and the one with independent signals are stable at about 56.3% and 95.7%, respectively. The area of the proposed 2T1R shared structure increases 1.9% compared to 1T2R, while it costs 20.1% less than that of 2T1R independent structure.

Figure 12. System-level Simulation for the Chip Area of Various Structures.

Figure 13 illustrates the tendency of increased energy consumption when memory capacity ranges from 512Kb to 1Gb. Compared with the 1T1R memory structure, the 1T2R structure has more than 34% energy consumption. Meanwhile, the energy consumption of 2T1R structure with shared signals and the one with independent signals have the stable increase about 68.7% and 83.8%, which is mostly due to the higher bias voltage of RESET. Specifically, the energy increment in 2T1R with shared signals is larger than the one with independent signals when storage capacity is small enough. Since the auxiliary peripheral circuits occupy less proportion of energy, and the H-tree networks occupy the most significant energy consumption in large-scale memory, the ratio of energy increment in proposed structure will be much less than the one with independent signals in more than 128Mb capacity. Besides the conventional read operation, the 1T2R structure introduces another detection phase, which is not included in the read operation of 2T1R structure. This simplification abates about 400pJ in energy consumption and 1ns in delay. The 2T1R structure eliminated the ceiling of normal read delay (2ns) in the RESET operation of the 1T2R structure.

Figure 13. System-level Simulation for the Energy Consumption of Various Structures.

5. Summary

In this paper, a compact memory structure based on 2T1R is proposed to alleviate the SEU influence on RRAM storage reliability. The proposed structure is modified based on the 2T1R structure with independent signals by flipping the cells to share the signals on horizontal dimension, and the auxiliary circuits are added to meet the requirement of signal selection and SEU protection in the new structure. The SPICE simulation shows that the proposed structure can successfully alleviate the SEU in RRAM array. The area of the 2T1R structure is merely 1.9% larger than that of 1T2R. Meanwhile, the 2T1R shared structure reduces the timing consumption and energy cost in both read operation (1ns, 400pJ) and RESET operation (2ns).

References