The Study of TSV-Induced and Strained Silicon-Enhanced Stress in 3D-IC

Jindong Zhou*, Youliang Jing, Pingqiang Zhou
School of Information Science and Technology, ShanghaiTech University, Shanghai, China
*Corresponding Author’s Email: zhoujd@shanghaitech.edu.cn

ABSTRACT
In this work, we discuss the influences of strained silicon technology on transistors in the context of TSV thermal stress. An accurate thermal stress distribution around a single TSV is firstly obtained by finite element analysis. Then we simulate the transistors using strained silicon technology and apply the TSV stress to the structure to study their magnitudes and mutual influences. It is demonstrated that the stress distribution combination of these two stress sources of planar transistors can be viewed as the superposition of the separate results. Finally, based on the updated stress distribution, the mobility variations of transistors around the TSV are studied.

INTRODUCTION
Three Dimensional Integrated Circuit (3D-IC) technologies have been proposed and transferred to products for several years because it has high integration density and potential high bandwidth due to stacking the dies vertically in one chip package. The key structure to serve as the interconnections between dies is Through Silicon Via (TSV), which is a copper pillar. TSVs go through the silicon substrates of one die and connect to another die to transmit signals or supply power. One application is the 3D NAND flash technology [1].
However, the manufacturing process of TSV will induce thermal stress in the die because of the mismatch of the Coefficient of Thermal Expansion (CTE) of materials, especially between the TSV (copper) and the substrate (silicon). What’s more, when there is stress in the substrate near TSVs where transistors are located, the characteristics (mobility and threshold voltage) of the transistors will be influenced [2].

As a result, it is necessary to study the stress distributions in a TSV based 3D-IC. Typically, there are three types of approaches to get the stress: one is the Finite Element Analysis (FEA) method [3], the second is the analytical method [4] and the last is the mixed semi-analytical method [2].

To the best of our knowledge, the existing works considered the TSV thermal stress together with Shallow Trench Isolation (STI) [5] or package components [6] and they used superposition to combine these parts to form the whole stress distributions. Besides the aforementioned structures in new processes, another stress source is bound to emerge, which is the strained silicon. This technology is firstly raised by Intel in 2002 [7]. Strained silicon can introduce extra stress in the channel of transistors to improve the electrical performance. In strain engineering, in addition to planar transistors, FinFETs are complex but benefit more from this technology.

In this work, we first get an accurate stress distribution of a complete single TSV 3D structure through FEA simulation. Then we launch simulations of strained-Si transistor structures to get the enhanced channel stress. The TSV induced thermal stress is added afterwards to identify whether they influence each other. The results prove that for planar transistors they can be added linearly. At last, we evaluate the transistor mobility variations around a TSV in 3D-IC. Typically, strained-Si technology can enhance the transistor mobility significantly, while the TSV induced thermal stress will cause mobility variations around it.

BACKGROUND
TSV induced thermal stress
At the beginning of the whole work, the TSV thermal stress needs to be figured out. We simulate a complete TSV 3D structure to get the thermal stress around it. Note that, all simulations mentioned in this work are launched by an FEA tool-ABAQUS and all data are processed by MATLAB. We choose FEA method to capture the stress distributions rather than the analytical methods because it can accurately catch the influences from all components in a complex 3D structure.

To simulate the thermal stress of a structure using FEA tools, a 3D model and related material parameters are required. We do the simulation in ABAQUS based on the structures shown in M. Jung’s work [3]. The related materials and parameters are listed in Table I. The temperature in simulation steps is set from 275°C to 25°C with reference to the real manufacturing process.

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (ppm/K)</th>
<th>Young’s modulus (GPa)</th>
<th>Poisson’s Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu</td>
<td>17</td>
<td>110</td>
<td>0.35</td>
</tr>
<tr>
<td>Si</td>
<td>2.3 ×10⁶</td>
<td>130</td>
<td>0.28</td>
</tr>
<tr>
<td>SiO₂</td>
<td>2.5 ×10⁵</td>
<td>71</td>
<td>0.16</td>
</tr>
<tr>
<td>LowK</td>
<td>20</td>
<td>9.5</td>
<td>0.3</td>
</tr>
<tr>
<td>Ti</td>
<td>8.6</td>
<td>116</td>
<td>0.32</td>
</tr>
<tr>
<td>Si0.4Ge0.2</td>
<td>7.549e-6</td>
<td>153.6</td>
<td>0.277</td>
</tr>
</tbody>
</table>

*: Virtual CTE used in Section ‘STRESS SIMULATION’

After simulation, the stress components near the substrate surface along the radius direction of the TSV are sampled. Then the stress distributions are generated in cloud chart form by interpolation in MATLAB. Three normal and one shear stress distributions are shown in Fig. 1, while the other two shear stress components are not shown because their magnitudes are so small that can be ignored.
Positive and negative stress values mean tensile and compressive stress respectively. All stress distributions can basically match the ones in work [3]. The peak stress component appears at the edge between the TSV and the substrate which is over 400MPa. The stress will decrease approximately exponentially along the radius. Generally, the stress may cause cracks in the die and destroy the circuit function.

Strained silicon technology

Strained silicon technology has been widely used in manufacturing process since it was proposed in 2002. The strained silicon transistors usually have special structures with special materials like SiGe or Si3N4 to introduce additional stress in the channel to improve the performance.

The strained PMOS structure with SiGe is taken as an example. Because of the lattice mismatch between substrate (Si) and source/drain (SiGe), a uniaxial compressive stress is induced in the region where the transistor channel lies. A schematic diagram is demonstrated in Fig. 2(a).

Results of strained silicon enhanced stress

The stress along the channel is shown in Fig. 2(b). The (x,y,z) directions are the channel length, channel width and height directions respectively. In addition, the three shear stress components are not shown because they are not large or critical enough for the following analysis.

$S_{xx}$, which is the normal stress component along the channel length direction, has a major impact on device performance. On average, $S_{xx}$ has about 350MPa compressive stress in the channel of the 45nm transistor. We observe that stresses have comparatively large changes at the ends of the channel. The reason is that these positions are near the interfaces of several different materials, which causes stress to vary. Also, the straight interfaces and sharp corners in the simulation structure make things worse, while in real devices, the phenomenon is mitigated due to the variations and limited precision of manufacturing process.

One thing should be clarified is that due to the different settings and parameters of materials and different structures of the strained silicon transistors, the stress results will differ. Our results are reasonable because they can match the order of magnitude of the ones mentioned in related works [10].

Results of the stress combination

In real circuit design process, the TSVs will be placed with the transistors around and the strained silicon technology is widely used in modern process. Then the stress distributions under this situation need to be studied. We apply an additional compressive stress field to the strained silicon transistor structure in simulations to serve as the TSV induced thermal stress $S_{xx}$ at a certain position.

As shown in Fig. 3, the whole $S_{xx}$ stress distribution of simulation results ($S$:Combination-sim.) can be seen as the superposition ($S$:Combination-theo.) of the TSV thermal stress ($S$:TSV, 130MPa here) and the strained silicon technology enhanced stress ($S$:Strained-Si) if ignoring the structure induced changes at both ends of the channel mentioned above. All other stress components as well as different TSV induced stresses at different positions around TSV have the same superposition feature. The intuitive
explanation is that these two stresses have separate causes and the stress itself can physically be added linearly in nature.

However, the FinFET case hardly shows the superposition feature. We speculate from our results that an explanation is that the FinFET has a complex 3D structure such that the TSV stress influences are somehow reduced by certain parts of the structures, which deserves further studying.

**INFLUENCE OF THE STRESS ON TRANSISTORS**

How these stress facts influence the electrical performance of the transistors is the key problem we concern about. Based on the theoretical formulas and parameters listed in Jaeger’s work [11], we can export the transistor mobility variations.

**Mobility variations around a TSV**

In semiconductors, the stress will affect the band gap, making the electrons easier or harder to leap to the conduction band. This is called the piezoresistive effect, which causes a change in mobility. Based on the formulas and the stress distributions mentioned above, the mobility variations of NMOs and PMOS around a TSV are shown in Fig. 4.

![Mobility variations around a TSV](image)

Note that, all transistor channels are assumed to locate along the X direction. It is observed that both PMOS and NMOS will be influenced by the TSV stress. NMOS suffers seriously. Although at a radius of 5um which is 2.5um away from the edge, the NMOS mobility variations are still very large (around 10%). One reason might be that the parameters from the reference work are out of date. From the perspective of today’s process, with heavily doped materials, the influences will be lighter.

**Mobility variations around a TSV with strained silicon**

Next, the 45nm strained silicon transistors are taken into consideration that we assume they can be placed everywhere around a TSV. Because of the property of superposition, all stress components from the TSV and the channel at a certain point can be simply added up. For simplicity, the average stress values in the channel from the results in Fig. 2(b) are used in calculation. It can be reasonable since the 45nm channel length is far smaller than the influence range of the TSV stress which is in um’s. Results are shown in Fig. 5. Compared with the PMOS results in Fig. 4, the strained silicon technology can raise the mobility by about 25%, which also basically matches the results from Intel [10].

Although the influence from the TSV is from -2% to 5%, which seems much smaller than the enhanced mobility from strained silicon, they cannot be ignored. One reason is that it will cause performance imbalances in circuit. When placing the transistors around the TSV in real circuit designs, those variations will cause circuit performance issues cumulatively like clock asynchrony and thermal imbalance.

**CONCLUSION AND FUTURE WORK**

This work intends to reveal the influences from TSV stress on strained silicon transistors. We study the channel stress enhanced by strained-Si technology based on the thermal stress distributions around a TSV. It is proved by simulation that for planar strained-Si transistors, the TSV stress can be added linearly. Finally, we discuss the mobility changes. It can be enhanced by strained-Si while the variations brought by TSV should also be treated carefully in design.

Actually, there are still many issues that are worth further researching. For example, the structure effects from complex 3D components like STI and FinFET in stress analysis need to be studied quantitatively.

**REFERENCES**