Yajun Ha

School of Information Science & Technology
ShanghaiTech University
393 Middle Huaxia Road
Shanghai, P. R. China

Tel: +86-21-20685371

Email: yajun_ha@hotmail.com

Education

Ph. D.	Electrical Engineering	Katholieke Universiteit Leuven, Belgium, 2004
M. Eng.	Electrical Engineering	National University of Singapore, Singapore, 2000
B. S.	Electrical Engineering	Zhejiang University, Zhejiang, China, 1996

Current and Previous Academic Positions

Jan. 2017 – Now	Professor School of Information Science & Technology ShanghaiTech University Shanghai, P. R. China Adjunct Associate Professor Department of Electrical and Computer Engineering National University of Singapore
Jan. 2014 – Jan 2017	Co-Director & Scientist I^2R-BYD Joint Lab Institute for Infocomm Research Agency for Science, Technology and Research Singapore Adjunct Associate Professor Department of Electrical and Computer Engineering National University of Singapore
Mar. 2004 – Dec. 2013	Assistant Professor Department of Electrical and Computer Engineering National University of Singapore
Jan. 1999 – Feb. 2004	Affiliate Researcher Design Technology Division IMEC, Belgium

Jul. 1997 – Jan. 1999	Graduate Research Assistant Department of Electrical Engineering National University of Singapore

Other Professional Experiences

Aug. 1996 – Jun. 1997	Research Engineer Institute of Telecommunication & Measurement and Control, Shanghai Aerospace Bureau, China

Research Interests

- Field Programmable circuits, architectures, design tools and applications
- Ultra low power digital system design and synthesis
- Embedded system architecture and design methodologies
- VLSI for cryptographic and video applications
- Smart and autonomous electric car related technologies

Research Grants

- Intelligent hardware design framework, Start-up Grant from ShanghaiTech University, Principal Investigator, RMB$5,000,000, 1/2017-1/2021.
- Autonomous Electric Vehicle Technologies, Industry Grant from BYD, Co-Principal Investigator, S$36,000,000, 11/2013-10/2019.
- A Power-Efficient Heterogeneous Architecture and Run-Time Manager for Data Center Servers, Singapore A*Star Grant, Principal Investigator, S$876,813, 08/2011~04/2013
- Secured Large Scale Shared Storage System, Singapore A*Star Grant, NUS Principal Investigator, in charge of S$709,092 out of total S$1,815,515, 08/2011~07/2014
- Co-PI of A*Star fund “Pseudo-Radom Single Photon Counting for Time-Resolved Optical Spectroscopy and Imaging”, R-397-000-035-305, start date: 15/07/2006, completion date: 31/12/2009, project amount S$635,140
- Co-PI of ARF fund “Global Virtual Machine”, R-263-000-213-112, start date: 01/11/2004, completion date: 31/01/2008, project amount S$92,365
- PI of ARF fund “Networked Reconfigurable Embedded Systems”, R-263-000-312-112, start date: 12/11/2004, completion date: 11/11/2007, project amount S$97,789.

Teaching Experience

- Conducted 3 undergraduate courses and 1 postgraduate course in the area of computer architectures, embedded system designs and reconfigurable computing. Develop two new courses from scratch.

- Graduated 9 PhDs and 7 MEng students so far, and supervising another 1 PhD and 1 Master students.
- Supervised several undergraduate students to won local and international awards.
- Fall 2004 – Spring 2013, EE 2007: Microprocessor Systems (8088/ARM)
- Fall 2012, 2014-2016, EE 6213: Reconfigurable Computing (new course developed)
- Every Spring 2005-2016, EE 4218: Embedded Hardware System Design (new course developed)
- Xilinx Authorized Trainer for the following courses:
    - Designing with VHDL
    - Advanced FPGA Design
    - Designing a LogicCORE PCI Express System
    - Designing with Ethernet MAC Controllers

Awards and Honors

- Y. Pu, J. Pineda, H. Corporaal and Y. Ha, "An Ultra Low-Energy/Frame Multi-standard JPEG Co-processor in 65nm CMOS with Sub/Near Threshold Power Supply", **Highlight Paper** in *Proc. of the ISSCC*, San Francisco, USA, Feb 2009.
- Lee, W. Loke, W. Zhang and Y. Ha, "Fast and Accurate Interval-Based Timing Estimator for Variability-Aware FPGA Physical Synthesis Tools", **Best Paper Nomination** in *Proc. the 17th FPL*, Amsterdam, the Netherlands, Aug 2007.
- **Best Poster Award** at 19th ProRISC, an annual Workshop on Integrated System and Circuits, in Veldhoven, Netherlands, 2008
- First place prize in the Philips Young Innovators Challenge 2005/2006 and a cash prize of S$10000. The win was featured in Business Times (29th May 2006), Straits Times Digital Life (30th June 2006) and Lianhe Zaobao.
- Loke Wei Ting, under my supervision won the second place in the student paper contest of IEEE region 8, 2007.
- The student teams that I supervised have won the Second and Third Class Prizes in 2004/2006/2008 Intel Cup Undergraduate Electronic Design Contest in Shanghai, China.
- Research Scholarship of IMEC, Belgium (1999–2004)
- Research Scholarship of National University of Singapore (1997-1999)

Professional Activities and Services

- Associate Editor, IEEE Transactions on Circuits & Systems I (2016-2017).
- Associate Editor, IEEE Transactions on VLSI Systems (2013 - 2014)
- Associate Editor, IEEE Transactions on Circuits & Systems II (2011-2013).
- Associate Editor, Journal of Low Power Electronics (JOLPE), 2009 – present
- Program Co-Chair of FPT 2013 and FPT 2010.
- General Co-Chair of ASP-DAC 2014.
- Chairman of Singapore Chapter, IEEE Circuits and System Society. (2011 and 2012)
- Steering Committee Member of ASP-DAC,
- Program Committee Members of DAC, DATE, ASP-DAC, FPGA, FPL, FPT, ARC, RAW, ERSA and HEART.
- Local Arrangement Chair of FPT 2005.

- Expert Group Member of Chinese National Electronic Design Contest (NUEDC) - Embedded System Design Invitational Contest (2006, 2008, 2010 and 2012)
- Senior member, IEEE (Since 2010).

University Services

- ECE Department M.Eng/PhD Program Manager, 2008 - 2010
- Member of Faculty Design Concentric Curriculum Committee, 2008 - 2010
- Member of Academic Committee of Computer Engineering Program, 2009 - now
- ECE Alumni Committee, 2009 – 2010
- Supervisor of PCB Lab, 2007-2013
- Supervisor of Digital Systems and Applications Lab, Since 2013

Proposal Review

- External proposal reviewer, Netherlands Science Foundation, 2007
- External research proposal reviewer, Qatar National Research Fund, 2009 and 2012, 2015

Student Advising

Current Graduate Students:

- Chin Hau Hoo, Ph.D. candidate (co-supervise with Dr. Akash Kumar)
- Ang Li, Ph.D. candidate (co-supervise with Dr. Akash Kumar)
- Anastacia Alvarez, Ph.D. candidate (co-supervise with A/P Massimo Alioto, Dr. Zhou Jun IME)

Graduated Students:

1. Akash Kumar, PhD, 2009, Chair Professor, Technical University of Dresden (TU/e/NUS Joint PhD with Profs H. Corporaal and B. Mesman)
2. Yu Pu, PhD, 2009, Research Scientist, Qualcomm Research Labs USA (NUS/TU/e Joint PhD with Profs J. Pineda and H. Corporaal)
3. Heng Yu, Ph.D, 2012, Assistant Professor, University of UAE (co-supervised with Prof. B. Veeravalli)
4. Xiaolei Chen, Ph.D., 2012, IC Design Senior Engineer, Intel Singapore, Singapore.
5. Do Thi Thu Trang, Ph.D., 2013, Institute for Infocom Research, Singapore (co-supervised with Dr. MT Le)
6. Wenfeng Zhao, PhD., 2014, Research Fellow, National University of Singapore
7. Rizwan Syed, Ph.D., 2014. (co-supervise with Prof. B. Veeravalli).
8. Junsong Hou, M.Eng, 2014, Research Engineer, NTU, Singapore.
9. Wei Ting Loke, M.Eng., 2012, Xilinx Singapore
10. Wenjuan Zhang, M.Eng, 2012.
11. Yanhui Li, M.Eng, 2008, Oracle, CA. USA
12. Jenn Yue Teo, M.Eng, 2008, DSO Lab, Singapore
13. Shefali Srivastava, M.Eng, 2007, HP Singapore

14. Chee Sing Lee, MEng, 2007, SPH Singapore

Publications

Book(s)

1. A. Kumar, H. Corporaal, B. Mesman and Y. Ha, "Multimedia Multiprocessor Systems: Analysis, Design and Management", 1st Edition, 163 pages, ISBN: 978-94-007-0082-6, by Springer, 2010.
2. Jinian Bian, Qiang Zhou, Peter Athanas, Yajun Ha, Kang Zhao: Proceedings of the International Conference on Field-Programmable Technology, IEEE FPT 2010, 8-10 December 2010, Tsinghua University, Beijing, China

Patents

1. Y. Ha, P. Schaumont, S. Vernalde and M. Engels, "Virtual hardware machine, methods, and device", US patent, No. 07150011, issued on 12 December, 2006.
2. Y. Ha, "Electric meter capable of avoiding or indicating fraudulent use of electricity", Chinese Patent, No. CN2144310U, issued in October 1993.

Journal Papers

1. Y. Wang and Y. Ha, “A DFA-Resistant and Masked PRESENT with Area Optimization for RFID Applications”, Accepted for publication in *ACM Transactions on Embedded Computing Systems*.
2. X. Wang, Y. Zhu, Y. Ha, M. Qiu and T. Huang, “An FPGA-Based Cloud System for Massive ECG Data Analysis”, Accepted for publication in *IEEE Transactions on Circuits and Systems II*.
3. M. Zhu, Y. Ha, C. Gu and L. Gao, “An Optimized Logarithmic Converter with Equal Distribution of Relative Errors”, *IEEE Transactions on Circuits and Systems II*， Vol 63, Issue 9, pp848-852, Sep 2016.
4. A. Li, A. Kumar, Y. Ha and H. Corporaal, “Correlation Ratio Based Volume Image Registration on GPUs”, *Microprocessors and Microsystems (MICPRO)*, Vol 39, Issue 8, pp998-1011, Nov 2015.
5. G. Jiang, J. Wu, Y. Ha, Y. Wang and J. Sun, “Reconfiguring Three-dimensional Processor Arrays for Fault-tolerance: Hardness and Heuristic Algorithms”, *IEEE Transactions on Computers*, Vol 64, Issue 10, pp2926-2939, Oct 2015.
6. W. Zhao, Y. Ha and A. Massimo, “Novel Self Body-Biasing and Statistical Design for Near-Threshold Circuits with Ultra Energy-Efficient AES as Case Study”, *IEEE Transactions on VLSI Systems*, Vol 23, Issue 8, pp1390-1401, Aug 2015.
7. W. Zhao, A. Alvarez and Y. Ha, “A 65-nm 25.1-ns 30.7-fJ Robust Subthreshold Level Shifter with Wide Conversion Range”, *IEEE Transactions on Circuits and Systems II*, Vol 62, Issue 7, pp671-675, July 2015.
8. T. Nguyen, Y. Wang, Y. Ha, R. Li, “Performance and Security-Enhanced Fuzzy Vault Scheme Based on Ridge Features for Distorted Fingerprint”, IET Biometrics, Vol 4, Issue 1, pp29-39, Mar 2015.

9. K. Huang, Y. Ha, R. Zhou, A. Kumar and Y. Lian, “A Low Active Leakage and High Reliability Phase Change Memory (PCM) based Non-Volatile FPGA Storage Element”, *IEEE Transactions on Circuits and Systems I*, Vol 61, Issue 9, pp2605-2613, Sep 2014.
10. Y. Wang and Y. Ha, “A Performance and Area Efficient ASIP for Higher-order DPA-resistant AES”, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol 4, Issue 2, pp190-202, June 2014.
11. H. Yu, Y. Ha, and B. Veeravalli, "Quality-Driven Dynamic Scheduling for Real-Time Adaptive Applications on Multiprocessor Systems", *IEEE Transactions on Computers*, Vol 62, No 10, pp2026-2040, Oct 2013.
12. T. Nguyen, Y. Wang, Y. Ha and R. Li, "Improved Chaff Point Generation for Vault Scheme in Bio-Cryptosystems", *IET Biometrics*, Vol 2, Issue 2, pp48-55, Jun 2013.
13. Y. Wang and Y. Ha, "FPGA Based 40.9 Gbit/s Masked AES with Area Optimization for Storage Area Network", *IEEE Transactions on Circuits and Systems II*, Vol 60, Issue 1, pp36-40, Jan 2013.
14. S. Rizwan, Y. Ha and B. Veeravalli, "A Low Overhead Abstract Architecture for FPGA Resource Management", *ACM SIGARCH Computer Architecture News (CAN)*, Vol 40, Issue 5, pp28-33, 2012.
15. A. Kumar, B. Mesman, H. Corporaal and Y. Ha, "Iterative Probabilistic Performance Prediction for Multi-Application Multi-Processor Systems", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol 29, Issue 4, pp538-551, Apr 2010.
16. Y. Pu, J. Pineda, H. Corporaal and Y. Ha, “An Ultra-Low-Energy Multi-Standard JPEG Co-Processor in 65nm CMOS with Sub/Near Threshold Supply Voltage”, *IEEE Journal of Solid-State Circuits*, Vol 45, Issue 3, pp668-680, Mar 2010
17. H. Tian, S. Fernando, H. Soon, Q. Zhang, C. Zhang, Y. Ha and N. Chen, "Ultra Storage Efficient Time Digitizer for Pseudo Random Single Photon Counter Implemented on Field Programmable Gate Array", *IEEE Trans. on Biomedical Circuits and Systems*, Vol 4, Issue 1, pp. 1-10, Feb 2010.
18. A. Kumar, S. Fernando, Y. Ha, B. Mesman and H. Corporaal, "Multi-processor Systems Synthesis for Multiple Use-Cases of Multiple Applications on FPGA", *ACM Transactions on Design Automation of Electronic Systems*, Vol 13, Issue 3, July 2008, pp. 1-27, ISSN:1084-4309.
19. J. Teo, Y. Ha and C. Tham, "Interference-Minimized Multipath Routing with Congestion Control in Wireless Sensor Network for High-Rate Streaming", *IEEE Trans. on Mobile Computing*, Vol. 7, No. 9, pp. 1124-1137, Sep 2008.
20. A. Kumar, B. Mesman, B. Theelen, H. Corporaal and Y. Ha, “Analyzing Composability of Applications on MPSoC Platforms”, *Journal of Systems Architecture*, Vol 54, Issue 3-4, March 2008, pp. 369-383, ISSN: 1383-7621.
21. Q. Zhang, H. SOON, H. Tian, S. Fernando, Y. Ha and N. Chen, "Pseudo-Random Single Photon Counting for Time-Resolved Optical Measurement". *Optics Express*, Vol 16, No. 17, pp. 13233-13239, August 2008.
22. J. Ng, C. Tan and Y. Ha, "An embedded system to support tele-medical activity". *International Journal of Software Engineering and Knowledge Engineering*, Vol 15, No. 2, pp. 271-278, 2005.
23. Y. Tan, A. Thampi, D. Sebastian and Y. Ha, "Design of seamless protocol switching layer for voice over internet protocol that switches between bluetooth and IEEE802.11". *International Journal of Software Engineering and Knowledge Engineering*, Vol 15, No. 2, pp. 279-286, 2005.

24. Y. Ha, S. Vernalde, P. Schaumont, M. Engels, R. Lauwereins and H. Man, "Building a virtual framework for networked reconfigurable hardware and software objects". *The Journal of Supercomputing*, Vol 21, No. 2, pp. 131-144, 2002.
25. Y. Ha, M. Li and A. Liu, "A new CMOS buffer amplifier design used in low voltage MEMs interface circuits". *Analog Integrated Circuits and Signal Processing*, 27, no. (1-2) pp. 7-17, 2001.

Conference Papers

1. Yi. Wang and Y. Ha, “High Throughput and Resource Efficient AES Encryption/Decryption for SANs”, in *Proc of 2016 IEEE Int'l Symposium on Circuits & Systems*, Montreal, Canada, May 22-26, 2016.
2. Yi. Wang and Y. Ha, “Improving Performance of Shuffled Higher-Order Masked AES via Instruction Extension”, in *Proc of FPT 2015*, New Zealand, Dec. 2015.
3. C. Hoo, A. Kumar and Y. Ha, “ParaLaR: A Parallel FPGA router based on Lagrangian Relaxation”, in *Proc. of FPL 2015*, London, United Kingdom, Aug 2015.
4. W. Zhao, M. Alioto and Y. Ha, “AES Architectures for Minimum-Energy Operation and Silicon Demonstration in 65nm with Lowest Energy Per Encryption”, in *Proc. of ISCAS 2014*, Lisbon, Portugal, May 2015.
5. Q. Wu, Y. Ha, A. Kumar, S. Luo and M. Haque, “A Heterogeneous Platform with GPU and FPGA for Power Efficient High Performance Computing”, in *Proc of ISIC 2014*, Singapore, Dec. 2014.
6. Y. Wang, A. Kumar and Y. Ha, “FPGA-based High Throughput XTS-AES Encryption/Decryption for Storage Area Network”, in *Proc of FPT 2014*, Shanghai, China, Dec. 2014.
7. W. Zhao, Y. Ha and Z. Yang, “A 0.4V 280-nW Frequency Reference-Less Nearly All-Digital Hybrid Domain Temperature Sensor”, in *Proc. of A-SSCC 2014*, Taiwan, Nov. 2014.
8. H. Yu, R. Syed and Y. Ha, “Thermal-Aware Frequency Scaling for Adaptive Workloads on Heterogeneous MPSoCs”, in *Proc. of DATE 2014*, Dresden, Germany, Mar. 2014.
9. J. Hou, H. Yu and Y. Ha, “The Architecture and Placement Algorithms for a Unidirectional Routing Based 3D FPGA”, in *Proc of FPT 2013*, Kyoto, Japan, Dec. 2013. (**Best Paper Candidate**)
10. Y. Chen, M. Felipe, Y. Wang, Y. Ha, S. Ren and M. Khin, “sAES A High Throughput and Low Latency Secure Cloud Storage with Pipelined DMA Based PCIe Interface”, in *Proc of FPT 2013*, Kyoto, Japan, Dec. 2013.
11. W. Loke, W. Zhao and Y. Ha, "Criticality-based Routing for FPGAs with Reverse Body Bias Switch Box Architectures", in *Proc of FPL 2013*, Porto, Portugal, Sept. 2013.
12. Y. Wang and Y. Ha, "FPGA Based ReKeying for Cryptographic Key Management in Storage Area Network", in *Proc of FPL 2013*, Porto, Portugal, Sept. 2013.
13. C. Hoo, Y. Ha and A. Kumar, "A Directional Coarse-Grained Power Gated FPGA Switch Box and Power Gating Aware Routing Algorithm",in *Proc of FPL 2013*, Porto, Portugal, Sept. 2013.
14. W. Zhao, Y. Ha, C. Hoo and A. Alvarez, "Robustness-Driven Energy-Efficient Ultra-Low Voltage Standard Cell Design with Intra-Cell Mixed-Vt Methodology", in *Proc of ISLPED 2013*, Beijing, Sept. 2013.
15. Y. Wang and Y. Ha, "An Area-Efficient Shuffling Scheme for AES Implementation on FPGA", in *Proc. of ISCAS 2013*, Beijing, May 2013.

16. Z. P. Ang, A. Kumar and Y. Ha, "High Speed Video Processing Using Fine-Grained Processing on FPGA Platform", in *Proc. of FCCM 2013*, Seattle, Washington, April 2013.
17. M. S. Haque, A. Kumar, Y. Ha, Q. Wu and S. Luo,"TRISHUL: A Single-pass Optimal Two-level Inclusive Data Cache Hierarchy Selection Process for Real-time MPSoCs", in *Proc. of the 18th ASP-DAC*, Jan 2013.
18. C. Wang, X. Li, X. Zhou and Y. Ha. "Parallel Dataflow Execution for Sequential Programs on Reconfigurable Hybrid MPSoCs". in *International Conference on Field-Programmable Technology*, Seoul, Korea, Dec. 10-12, 2012.
19. V. Y. Khoo and Y. Ha, "Link Aggregate Traffic Trend Prediction Based on Multiple Data-Driven Traffic Predictions for Pseudo-Adaptive Routing in Network-on-Chip", in *Proc. of HEART 2012*, Okinawa, Japan, May 2012.
20. W. Loke, Y. Ha and W. Zhao, "A Power and Cluster-Aware Technology Mapping and Clustering Scheme for Dual-VT FPGAs", in *Proc. of RAW 2012*, Shanghai, May 2012.
21. W. Loke and Y. Ha, "A Routing Architecture for FPGAs with Dual-VT Switch Boxes and Logic Clusters", in *Proc. of ARC 2012*, Hong Kong, Mar. 2012.
22. W. Loke and Y. Ha, "Power-aware FPGA Technology Mapping and CAD for Programmable-VT Architectures", in *Proc. of 20th ACM International Symposium on FPGAs*, CA, USA, Feb. 2012.
23. M. Zhu, J. Xiao, W. Wanggen and Y. Ha, "Error Flatten Logarithm Approximation for Graphics Processing Unit", in *Proc. of the 23rd International Conference on Microelectronics*, Tunisia, Dec. 2011.
24. W. Zhang and Y. Ha, "A Hilbert Curve-Based Delay Variation Characterization Method for FPGAs", in *Proc. of ISCAS 2011*, Rio de Janeiro, Brazil, May 2011.
25. Z. Yang, A. Kumar and Y. Ha, "An Area-efficient Dynamically Reconfigurable Spatial Division Multiplexing Network-on-Chip with Static Throughput Guarantee", *in Proc. of 2010 International Conference on Field Programmable Technology*, Beijing, China, Dec 2010.
26. W. Zhang, S. Srivastava and Y. Ha, "B*-Tree based Variability-Aware Floorplanning", *in Proc. of 2010 IEEE Asia Pacific Conference on Circuits and Systems*, Kuala Lumpur, Malaysia, Dec 2010.
27. H. Yu, B. Veeravalli and Y. Ha, "Leakage-Aware Dynamic Scheduling for Real-Time Adaptive Applications on Multiprocessor Systems", in *Proc. of 47th DAC 2010*, Anaheim, CA, USA, Jun 2010.
28. H. Yu, Y. Ha and B. Veeravalli "Communication-Aware Application Mapping and Scheduling for NoC-Based MPSoCs", in *Proc. of ISCAS 2010*, Paris, France, May 2010.
29. S. Rizwan, X. Chen, Y. Ha and B. Veeravalli "sFPGA2 - A Scalable GALS FPGA Architecture and Design Methodology", in *Proc. of the 19th FPL*, Prague, Czech, Aug 2009.
30. G. Zhu, H. Yu, Y. Ha and Y. Wang, "A Multi-Application Mapping Framework for Network-on-Chip Based MPSoC: An FPGA Implementation Case Study", *in Proc. of ERSA 09*, Las Vegas, USA, Jul 2009.
31. Y. Pu, J. Pineda, H. Corporaal and Y. Ha, "An Ultra Low-Energy/Frame Multi-standard JPEG Co-processor in 65nm CMOS with Sub/Near Threshold Power Supply", in *Proc. of the ISSCC*, San Francisco, USA, Feb 2009. (Highlight Paper)
32. P. Meher, Y. Ha and C. Lee, "An Optimized Design of Serial-Parallel Finite Field Multiplier for GF(2^m) Based on All-One Polynomials", in *Proc. of the 14th ASP-DAC*, Yokohama, Japan, Jan 2009.
33. J. Lim, E. Siow, Y. Ha and P. Meher, "Providing Both Guaranteed and Best Effort Services Using Spatial Division Multiplexing NoC with Dynamic Channel Allocation and Runtime

Reconfiguration", Accepted for publication in *Proc. of the 20th International Conference on Microelectronics*, Sharjah, UAE, Dec 2008. (Invited Paper)

34. Y. Pu, J. Pineda, H. Corporal and Y. Ha, "Towards Reliable and Ultra Low Energy Digital Circuits with Sub/Near Threshold Supply Voltage", in *Proc. of the 19th ProRISC*, Veldhoven, Netherlands, Nov 2008. **(Best Poster Award)**
35. S. Fernando, X. Chen and Y. Ha, "sFPGA - A Scalable Switch based FPGA Architecture and Design Methodology", in *Proc. of the 18th FPL*, Heidelberg, Germany, Sep 2008.
36. H. Liu, X. Chen and Y. Ha, "An Architecture and Timing-Driven Routing Algorithm for Area-Efficient FPGAs with Time-Multiplexed Interconnects", in *Proc. the 18th FPL*, Heidelberg, Germany, Sep 2008.
37. F. Wong and Y. Ha, "A Low Overhead Fault Tolerant FPGA with New Connection Box", in *Proc. of the 18th FPL*, Heidelberg, Germany, Sep 2008.
38. H. Tian, S. Fernando, H. W. Soon, Y. Ha and N. G. Chen, "Design of a High Speed Pseudo-Random Bit Seqenuce Based Time Resolved Single Photon Counter on FPGA", in *Proc. the 18th FPL*, Heidelberg, Germany, Sep 2008.
39. S. Fernando, H. Tian, H. SOON, Y. Ha and N. Chen, "Design of High Speed Pseudo Random Number Generator and Data Reconstruction Unit for DOT on FPGA", in *Proc. of OWLS10 Biophotonics Asia 2008*, Singapore, Aug 2008.
40. Y. Li, S. Fernando, H. Yu, X. Chen, Y. Ha and T. Tay, "Tighter WCET Analysis of Input Dependent Programs with Classified-Cache Memory Architecture", in *Proc. of the 15th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Malta, Aug 2008.
41. H. Liu, X. Chen and Y. Ha, "An Area-Efficient Timing-Driven Routing Algorithm for Scalable FPGAs with Time-Multiplexed Interconnects", in *Proc. of FCCM'08*, CA, USA, April 2008.
42. Y. Pu, J. Pineda, H. Corporaal and Y. Ha, "Statistical Noise Margin Estimation for Sub-Threshold Combinational Circuits", in *Proc. of the 13th ASP-DAC*, Seoul, South Korea, Jan 2008.
43. H. Yu, B. Veeravalli and Y. Ha, "Dynamic Scheduling of Imprecise-Computation Tasks for Maximizing QoS under Energy Constraints for Embedded Systems", in *Proc. of the 13th ASP-DAC*, Seoul, South Korea, Jan 2008.
44. P. Gade, R. Raily and Y. Ha, "A Branch Target Instruction Prefetching Technique for Improved Performance". In *Proc. of the 15th international Conference on Advanced Computing and Communications*, India, Dec 2007.
45. J. Teo, Y. Ha and C. Tham, "Interference-Minimized Multipath Routing with Congestion Control in Wireless Sensor Network for Multimedia Streaming", in *Proc. of MILCOM 2007*, Orlando, USA, Oct 2007.
46. R. Paily, V. Badam and Y. Ha, "Floating Gate Interferences on Vth Distribution In Eight Level High Density Flash Memory". In *Proc. of VLSI Design and Test Symposium 2007*, Kolkata, India, Aug 2007.
47. A. Kumar, S. Fernando, Y. Ha, B. Mesman and H. Corporaal, "Multi-processor System-level Synthesis for Multiple Applications on Platform FPGA", in *Proc. the 17th FPL*, Amsterdam, the Netherlands, Aug 2007.
48. C. Lee, W. Loke, W. Zhang and Y. Ha, "Fast and Accurate Interval-Based Timing Estimator for Variability-Aware FPGA Physical Synthesis Tools", in *Proc. the 17th FPL*, Amsterdam, the Netherlands, Aug 2007. (**Best Paper Nomination**)
49. Y. Pu, J. Pineda, H. Corporaal and Y. Ha, "VT Balancing and Device Sizing Towards High Yield of Sub-threshold Static Logic Gates", in *Proc. ISLPED 2007*, Portland, Oregon, USA, Aug 2007.

50. Dong, B and Y Ha, "Statistical Static Timing Analysis for Variability-Aware Latch-based Pipeline with Fuzzy Logic". In *Proc. of IPS Workshop*, Taiwan, Jul 2007.
51. W. Zhang and Y Ha, "Interval Arithmetic Based Variability-Aware Floorplanner". In *Proc. of IPS 2007*, Taiwan, Jul 2007.
52. A. Kumar, B. Mesman, H. Corporaal, B. Theelen and Y. Ha, "A Probabilistic Approach to Model Resource Contention for Performance Estimation of Multifeatured Media Devices", in *Proc. of the 44th DAC*, San Diego, USA, Jun 2007.
53. Z. Ye, S. Fernando, Y. Ha and N. Chen, "A fast and efficient Encryption Engine with Partial reconfiguration". In *Proc. of ICITA 2007*, Harbin, China, Jan 2007.
54. A. Kumar, B. Mesman, B. Theelen, H. Corporaal and Y. Ha, "Resource Manager for Non-preemptive Heterogeneous Multiprocessor System-on-chip". In *Proc. of the 4th Workshop on Embedded Systems for Real-Time Multimedia*, Seoul, South Korea, Oct 2006.
55. A. Kumar, B. Mesman, H. Corporaal, J. Meerbergen and Y. Ha, "Global Analysis of Resource Arbitration for MPSoC". In *Proc. of the 9th Euromicro Conference, DSD 2006*, Croatia, Sep 2006.
56. Y. Pu, C. Lee, Y. Ha and H. Corporaal, "POWER-EFFICIENT FPGA SWITCH WITH RECONFIGURABLE BUFFERS". In *Proc. of IPS* 2006, Taipei, Taiwan, Jul 2006.
57. Y. Pu and Y. Ha, "An Automated, Efficient and Static Bit-width Optimization Methodology Towards Maximum Bit-width-to-Error Tradeoff With Affine Arithmetic Model", in *Proc. the 11th ASP-DAC*, Japan, Jan 2006.
58. C. Lee and Y. Ha, "Design Space Exploration for Arbitrary FPGA Architectures". In *Proc. of ICESS 2005*, Xi'an, China, Dec 2005.
59. I. Ovadia, Y. Ha and H. Corporaal, "Using Multiple Paths in NoCs for Guaranteed Resource Allocation and Improved Best Effort Performance". In *IEEE Proc. of ProRISC 2005*, Veldhoven, Netherlands, Nov 2005.
60. S. Devinda and Y. Ha, "Design of networked reconfigurable encryption engine". In *Proc. of the 2005 IEEE Symposium on Field-Programmable Custom Computing Machines*, California, United States, Apr 2005.
61. Y. Ha, R. Hipik, S. Vernalde, D. Verkest, M. Engels, R. Lauwereins and H. Man, "Adding Hardware Support to the Hotspot Virtual Machine". *Lecture Notes in Computer Science 2438*, In *Proc. of FPL 02*, Montpellier, France, Sep 2002.
62. F. Chollet, A. Liu, X. Zhang, B. Zhao, V. Murukeshan, Y. Ha, L. Zheng, A. Asundi and G. Hegde, "Optical MEMS activities at the MicroMachines Centre, School of MPE, NTU in Singapore". In *Proc. of the Seiken symposium on Micro/Nano Mechatronics*, Tokyo, Japan, May 2002. (Invited paper)
63. Y. Ha, B Mei, P Schaumont, S Vernalde, R Lauwereins and H De man, "Development of a design framework for platform-independent networked reconfiguration of software and hardware". In Proc. of *FPL '01*, pp.264-274, Belfast, UK, Aug 2001. (LNCS 2147).
64. Y. Ha et al "A SW/HW interface API for java/FPGA co-designed applets". In *Proc. of FCCM'01*, CA, USA, April 2001.
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