DESIGN AND OPTIMIZATION OF ON-CHIP VOLTAGE REGULATORS FOR HIGH PERFORMANCE APPLICATIONS

[**Invited Special Session Paper**][1]

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ABSTRACT

Voltage regulators are traditionally fabricated off-chip because they rely on bulky energy storage devices on the board. Recent progress shows that it is possible to integrate such voltage regulators on chip to improve voltage regulation, and to potentially provide better support for DVFS technique to reduce power consumption in high performance multicore applications. This paper presents an overview of the design and optimization of on-chip voltage regulators for multicore applications.

INTRODUCTION

Power is a major challenge in current and future multicore processor design, and the dynamic voltage and frequency scaling (DVFS) technique has been widely used to reduce power consumption in recent high-performance multicore processors [1]–[3]. The varying performance demands in the cores of a multicore processor can be best met if DVFS is supported by providing wide range of VDD supply from the power delivery network.

Most conventional DVFS systems are based on off-chip voltage regulators driving on-chip power grids, which comes at the cost of additional complexity and area, since voltage regulators are built traditionally in board-level with large inductors or capacitors. The costs and sizes of such bulky modules severely limit their use for on-chip voltage regulation. In addition, due to the slow response time of the off-chip regulators, the DVFS control algorithms have to work on coarse temporal granularity, with voltage changes on the order of several microseconds [4], [5]. To enable fast (on the order of tens of nanoseconds) and fine-granularity (at the core or block level) DVFS, it is essential to develop fully integrated on-chip voltage regulators, which can significantly improve on-chip voltage regulation and eliminate load-transient spikes [6].

Power efficiency is one of the most critical design metrics for voltage regulators. The power efficiency of a regulator can be defined as the ratio of the power delivered to the load to the power extracted from the input source, i.e.,

$$\eta = \frac{V_{out}I_{out}}{V_{in}I_{in}} \quad (1)$$

The key challenge associated with realizing on-chip integrated regulators is the difficulty in achieving high efficiency at high power densities required by high-performance multicore applications. Due primarily to the lack of dense, high-quality-factor energy storage elements, on-chip voltage regulators are historically infeasible for high-performance applications, and they are limited to be used in ultra-low power applications (on the order of micro watts) [7], [8]. The need for multiple supply voltages in high performance multicore applications leads to several recent efforts in exploring fully integrated on-chip voltage regulators. Part of them focus on the design aspects of the voltage regulators, for example, how to design the internal structure of a regulator so that it can provide a wide range of supply voltage [9]–[12]. Others look at the application of these on-chip voltage regulators in multicore systems and present approaches to optimize the efficiency of the whole power delivery system integrating the on-chip voltage regulators (see Figure 1) [6], [13]–[15].

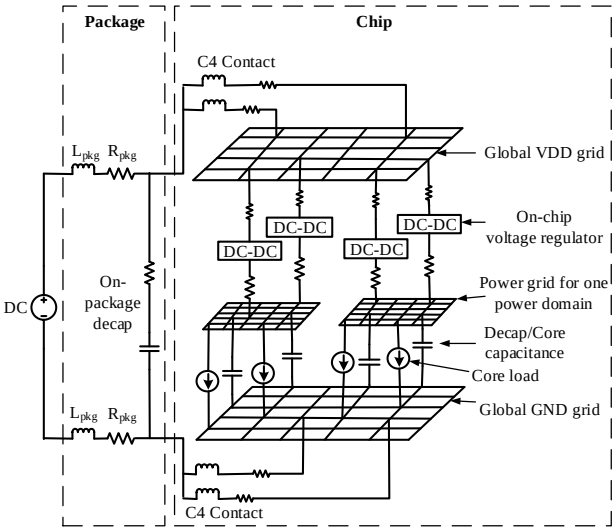

Figure 1: A power delivery system model integrated with on-chip voltage regulators [6].

[1] This paper is invited by Special Session of "Advanced CAD Techniques for Power/Temperature-Aware IC Design" in ICSICT 2014.

DESIGN OF ON-CHIP VOLTAGE REGULATORS

There are two kinds of typical voltage regulators – linear regulators and switching converters. Current-day voltage regulators are mostly implemented by linear regulators, such as LDOs [13], [16]–[18], but only switching converters can provide a wide range of output voltage at high efficiency which is critical for the application of DVFS in multicore systems [9], [19].

Linear Regulators

A linear regulator maintains a steady output voltage by varying its resistance in accordance with the load condition. Figure 2 shows the most efficient form of linear regulators – a low-dropout (LDO) voltage regulator which consists of a pass element (M_p), sampling resistors (R_{f1} and R_{f2}), reference voltage (V_{ref}), an error amplifier, and a differentiator [13], [17].

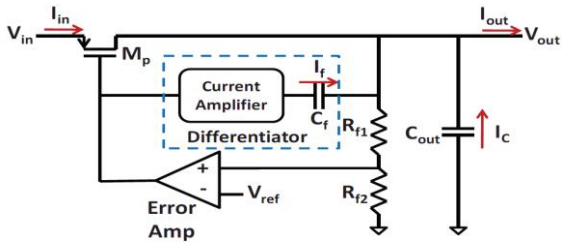

Figure 2 A LDO voltage regulator [17].

The dropout voltage V_{drop} of a linear regulator is defined as the minimum voltage drop across the regulator, i.e., the input-to-output differential voltage V_{in-out}, to maintain output voltage regulation. If V_{in-out} is less than V_{drop}, the regulator works in the dropout (linear) region and the output voltage decreases in proportion to the decreasing input voltage. In contrast, if V_{in-out} is larger than dropout voltage, the regulator is in regulation region and it maintains the output voltage at a stable level through the closed-loop feedback system consisting of the sampling resistors R_{f1} and R_{f2} and the error amplifier. Conventional LDO voltage regulators require a bulky off-chip output capacitor to ensure AC stability and load transient response. Recent work [17] proposed to add an auxiliary fast loop ("differentiator" in Figure 2) to provide a fast transient detector path as well as internal AC compensation.

The efficiency of an LDO is given by

$$\eta = \frac{V_{out}\, I_{out}}{V_{in}(I_{out} + I_{quies})} \qquad (2)$$

where I_{quies} is the quiescent current in the internal circuitry of the LDO that flows to the ground. From Equation (2) we can see that, to improve the efficiency of a LDO regulator

1) we should minimize the dropout voltage V_{drop} (which limits max V_{out}) and quiescent current I_{quies}. This can be achieved by improving the design of the LDO regulators [17], [20].
2) we should minimize the input-to-output differential voltage V_{in-out}. The larger V_{in-out} is, the lower the efficiency of the LDO is. This means that LDO regulators are not suited for DVFS applications that require a wide range of supply voltage.

Switching regulators

A switching regulator uses an active device that switches on and off to maintain an average value of output current. The active device can be an inductor or a capacitor.

Inductive (switched-model) DC-DC converter: A typical inductive switching regulator (also known as buck converter) is shown in Figure 3, which consists of switching power transistors, the output filter inductor (L_{out}) and capacitor (C_{out}), and a feedback control comprised of a hysteretic comparator and associated filter elements (C_{filter} and R_{filter}) that enhance loop stability.

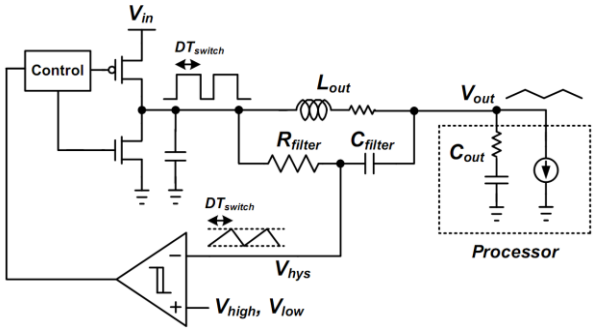

Figure 3 Inductive switching converter [4].

The power transistors acts as an inverter that switches on and off at a frequency and provides a square wave to the low-pass output filter. The regulator output voltage, V_{out}, is approximately set by the duty cycle of the square wave. V_{hys}, the output of the filter, is fed to the hysteretic comparator, whose output then sets the duty cycle of the square wave input to the power transistors. The hysteretic comparator has a high threshold V_{high} and a low threshold voltage V_{low}. When V_{hys} falls below V_{low}, the PMOS power switch turns on, and when the V_{hys} increases above V_{high} the NMOS turns on. Since V_{hys} is directly affected by V_{out}, hysteretic control can react very quickly when V_{out} fluctuates in response to load current transients [4].

In real design, parallel sets of power transistors and inductors can be interleaved and connected to the same output load such that the current through each inductor is interleaved across even time intervals. In this way, the interleaved inductor currents cancel out at the output and result in an average current with small ripple [4], [21].

The inductive DC-DC converters can achieve high efficiency and also work with large output load [10]. However, one big problem is that the *on-chip* inductive switching converters for high-performance applications require large inductors that are implemented on the metal

layers on chip, which may cause severe noise interference and special shielding process is needed for such inductors.

Switched-capacitor (SC) DC-DC converter: A SC converter (also known as charge pump) is a network of charge-transfer capacitors and switches that operates in two or more phases, converting an input voltage V_{in} to an output V_{out}. If V_{out} is higher than V_{in}, the conversion is called a "step-up" conversion. Vice versa, if If V_{out} is lower than V_{in}, the conversion is called a "step-down" conversion.

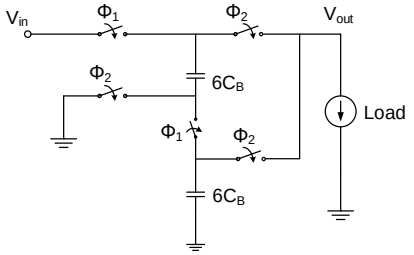

Figure 4 A 2:1 SC converter [6].

Figure 4 shows a SC converter with 2:1 conversion ratio (for clarity, the control unit and closed-loop feedback system is not shown). Two capacitors each with capacitance of $6C_B$ and five switches are connected in a network, and the switches are controlled by two signals Φ_1 and Φ_2. In the charging phase, Φ_1 turns ON two switches connecting the two charge-transfer capacitors in series. Since both capacitors have the same value of capacitance $6C_B$, each will be charged to $V_{in}/2$ if enough time is provided for the capacitors to be fully charged. In the discharging phase, three other switches turn ON, while the ones controlled by Φ_1 turn OFF. This will connect both capacitors in parallel with the output load, resulting in an output voltage $V_{out} = V_{in}/2$. As current starts to flow into the load, the charge stored in the capacitors will deplete and the output voltage will drop to $V_{in}/2 - \Delta V$ at the end of this stage before it is recharged in the next phase. The ripple ΔV at the output of the SC converter can be effectively controlled by multi-phase interleaving technique, and 16 and 32 phases are typically used in real designs.

A promising feature of SC converter is that, with the same total amount of flying capacitance, we can dynamically reconfigure the network of the capacitors and switches such that a SC converter can work with different conversion ratios at different times, so as to provide a wide range of supply voltage to support DVFS applications [9], [14], [15].

Recent works [11], [12] demonstrate that, with advanced design techniques and energy storage devices such as deep trench capacitors, a SC DC-DC converter can provide high power density (up to 2.3A/mm^2) and high efficiency (>80%), and therefore make itself a compelling candidate for high performance applications.

OPTIMIZATION OF ON-CHIP VOLTAGE REGULATORS

Recently there have been several pioneering works on the optimization of on-chip voltage regulators, with the aim of maximizing the power efficiency either at the regulator level [12] or at the system level [13], [15].

Zeng et.al. [13] have looked at the analysis and optimization of LDOs in a power delivery system with multiple power domains. They first develop a GPU-CPU simulation engine for a power delivery network with integrated LDOs, and then propose a simulation-based nonlinear optimization strategy to maximize the efficiency of the power delivery system by optimizing the number of the used LDOs for each power domain.

The work in [12] has presented models for the power loss inside the SC converters and focused primarily on optimizing the internal design of the SC converter to reduce wasted power *within the converter*, by controlling the voltage ripple ΔV and choosing the optimal switch width and switching frequency. Under this paradigm, the burden of optimizing the other power loss terms in the system, such as the voltage droop in the power grid (see Figure 1), is placed on conventional means for power delivery optimization [22].

The work [15] has studied the application and optimization of SC converters for DVFS in multicore power delivery system that may have multiple power domains. First, they suggest the use of distributed SC converters in a multicore system with multiple power domains. Their simulation results show that the voltage droop seen by the core loads is affected by both the number and location, i.e., distribution, of the converters. Compared to a single lumped converter, distributed converters with the same total amount of capacitance can significantly reduce the voltage droop by providing better localized voltage regulation. Second, they consider a holistic optimization of the SC converters *at the system level* to minimize the power loss in the whole power delivery system. Due to the fact that the current distribution in a multicore system is spatially imbalanced, using SC converters with identical size and evenly distributing them over a chip area is not the best choice. Therefore, they develop an accurate power loss model for the whole power delivery system integrated with SC converters, and then propose an ideal mathematical-programming-based CAD approach to automate the design and distribution of the SC converters supporting DVFS in a multicore system, with the objective of maximizing the efficiency of the whole power delivery system.

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